

UC3573 Buck Regulator PWM Control IC

**Typical Application Circuit for +12VDC Input to +5VDC/1A Output
Also : Demonstration Kit Circuit Schematic and List of Materials**

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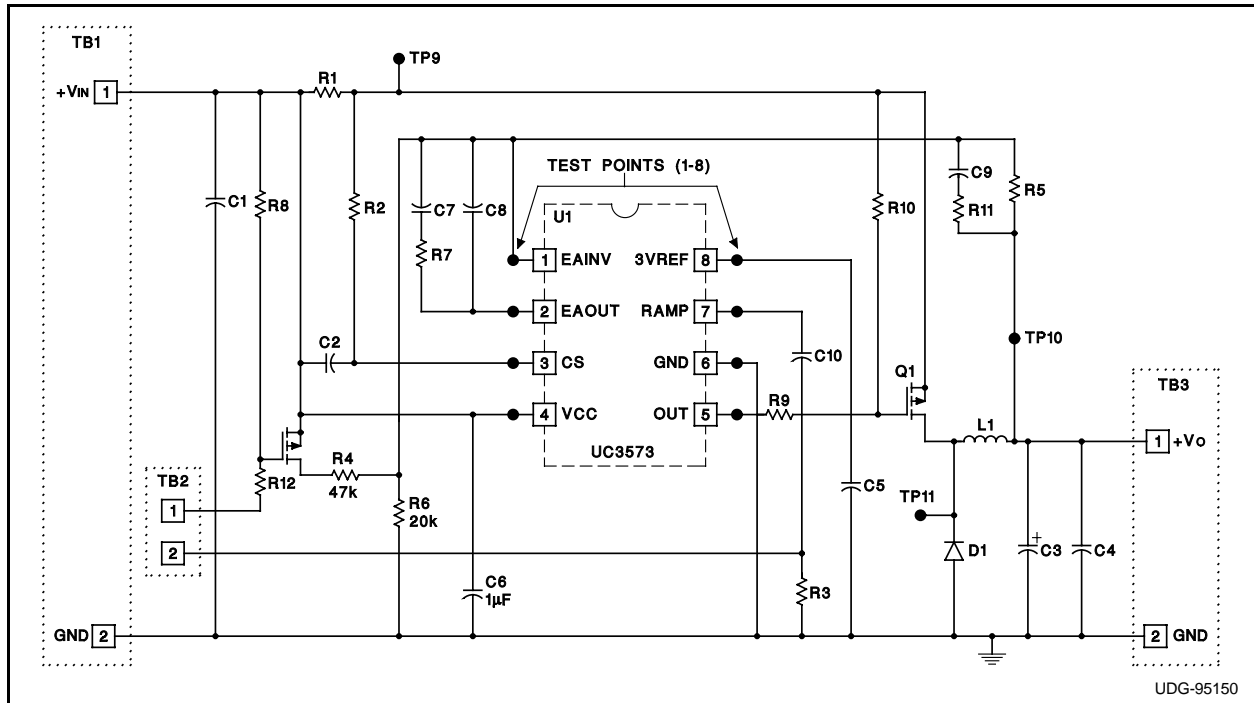


Figure 1. UC3573 Application Circuit Schematic

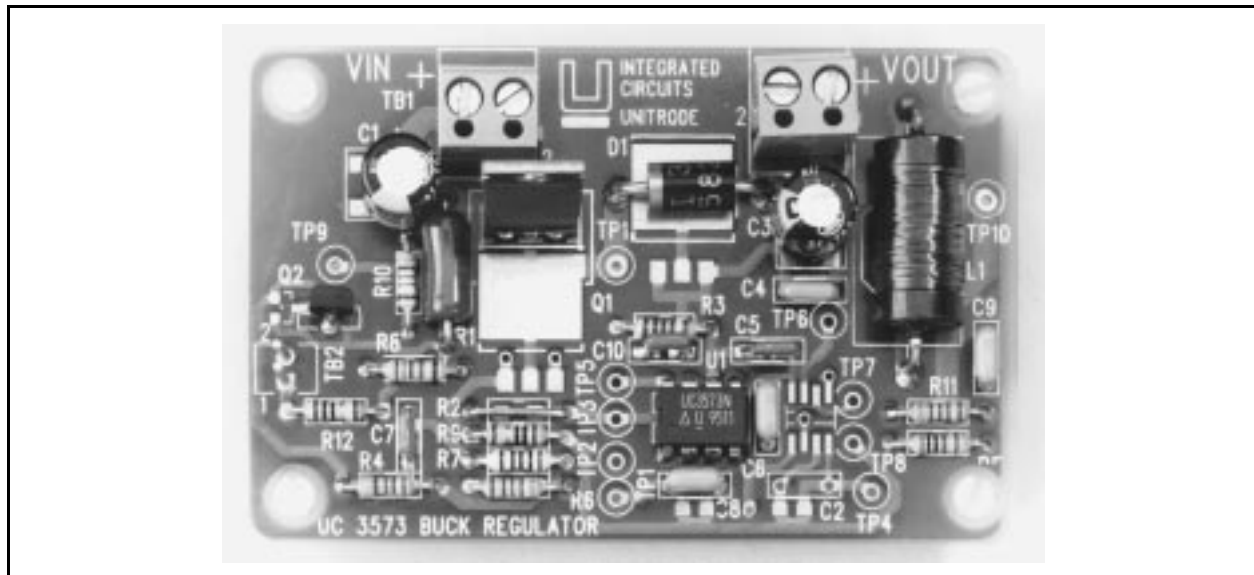


Figure 2. Photo of UC3573 Demo Kit

List of Materials:**Reference Value and Type**

C1,C3	CAP 82 μ F/25V Electrolytic, ESR < 0.25 Ω @100kHz (Panasonic HFQ or FA series)
C2	Not Used - Open Circuit
C4,C5	CAP 0.1 μ F/50V Ceramic
C6	CAP 0.47 μ F/50V Ceramic
C7	CAP 2.2nF/50V Ceramic NPO Type
C8	CAP 27pF/50V Ceramic NPO Type
C9	CAP 1.8nF/50V Ceramic
C10	CAP 680pF/50V Ceramic
D1	1N5820 3A/20V Schottky Diode
H1*	Heatsink for Q1
L1	220 μ H/2A : Coilcraft PCH-45 Series
Q1	IRF9Z30 P-Channel Power MOSFET, -50V, 0.2 Ω RDS(on)
Q2	BS250P P-Channel Signal MOSFET, -45V, 100 ohm RDS(on)
R1	0.27 Ω /1 Watt
R2	Short Circuit - Use AWG#22 Wire
R3, R9	20 Ω , 1/4W
R4	47k, 1/4W
R5	47k, 1/4W, 1%
R6	20k, 1/4W, 1%
R7	130k, 1/4W
R8, R10	100k, 1/4W
R11	7.5k, 1/4W
R12	200k 1/4W
TB1, TB3	Terminal Block
U1	UC3573 PWM

* = Optional

Test Equipment needed:

Power supply +12VDC/2A max.

Adjustable load for 5VDC/2A max.

Digital Multimeter 100 Ω , 1 Watt load resistor Oscilloscope.

Testing Procedure

1. Before applying power to the UC3573 Demo Kit, connect A 100 Ω preload resistor across the UC3573 output terminals at TB3. This places a minimum load of 50 milliamps on the +5VDC output of the converter to keep the Buck regulator inductor current continuous. Also connect the adjustable electronic or resistive load across the same output terminals. Set the load to draw no

current and observe correct \pm polarity when using an electronic load. Pin 1 of TB3 is the positive output (+) and pin 2 is the negative (-) terminal, or ground. Also connect the digital multimeter to the output terminals to measure the output voltage.

2. Connect the 12VDC/2A power supply to the UC3573 Demo Kit input terminal block observing the correct polarity. Pin 1 of TB1 is the positive input (+12VDC) and pin 2 is the return connection (-) and ground.
3. The oscilloscope and digital multimeter can be used to observe and measure signals at numerous nodes in the Buck converter. Test points TP1 through TP8 correspond directly to the respective pins of the UC3573 IC; ie. TP1 is the voltage at the UC3573's pin 1 with respect to ground. The various waveforms and amplitudes of the IC pins can be monitored over the operating ranges of input voltage and output current. Test points TP9 through TP11 are for further probing of the power stage.
4. Once all of the connections to the UC3573 demo kit have been verified, the +12VDC input can be applied. The output voltage of the Demo Kit should be approximately 5.0 VDC (4.8 to 5.2 VDC worst case) initially. Note that 1% tolerance resistors are used in the voltage divider network to the IC's error amplifier and the IC's internal reference voltage (Pin 8) has an initial tolerance of \pm 2%.
5. Gradually increase the load on the UC3573 Demo Kit output until the output voltage decreases to 4.5VDC or lower. Load current will be limited to approximately 1.3ADC, and decreasing the load resistance will only lower the output voltage, and not cause a significant increase in the converter's output current. This is a typical exhibition of the overcurrent protection feature of the IC. Each switching cycle, the pulse width output of the IC is turned off early (before the normal pulse width is reached) to reduce the input power drawn. This feature reduces the MOSFET switch power dissipation and provides protection from a short circuited or severely overloaded output condition. Once the fault has been removed, the output voltage will automat-

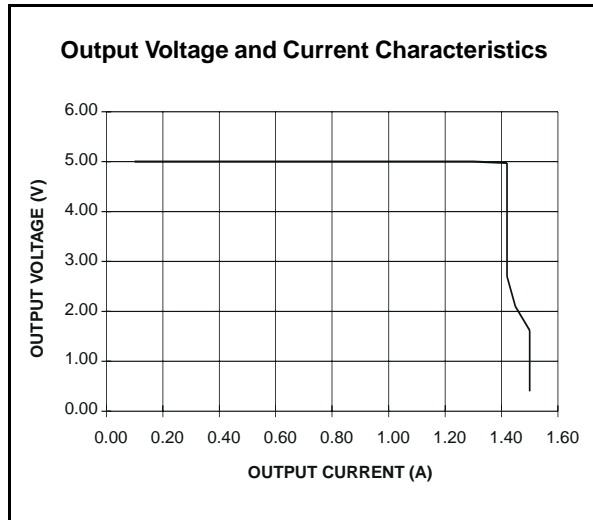


Figure 3. Converter Output Voltage Versus Current

ically return to the normal 5VDC amplitude. The exact profiles of output voltage versus output current is shown in Figure 3, and input power versus output power during overload conditions is shown in Figure 4.

Optional Features

Synchronization: Terminal block TB2 is for optional external synchronization of the UC3573 and for remote shutdown of the UC3573 Demo Kit. The required SYNC pulse input to TB2 (pin 2) is a brief pulse of approximately 1 volt amplitude. This adds to the IC's normal oscillator timing sawtooth waveform (RAMP, pin 7) to force the total waveform above the oscillator's internal upper threshold. Doing this will terminate the immediate switching cycle and initiate the next clock cycle. It is necessary that the synchronization frequency is higher than the UC3573 programmed oscillator frequency in order for this to work properly. Note that a low impedance, fairly high current drive circuit is required to force synchronization. More complete details can be found in Unitrode Application Note U-111 in the "Synchronization" section.

Remote Shutdown: The UC3573 controller can be placed into a low current (50 μ A typical)

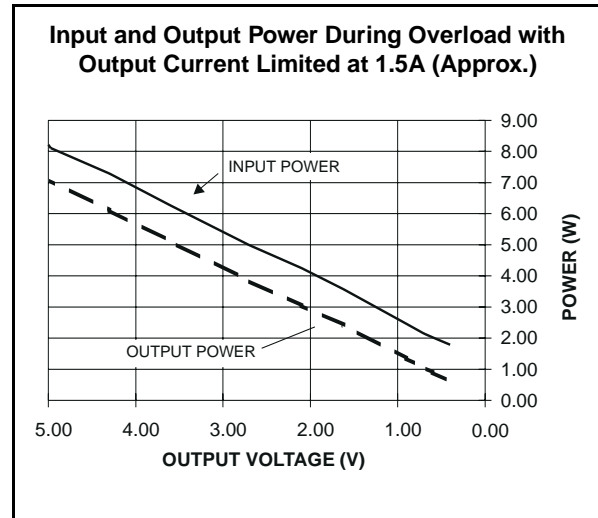


Figure 4. Converter Input and Output Power During Overload

standby mode by forcing the error amplifier inverting input above 2.6VDC. The circuitry used to facilitate this on the Demo Kit consists of transistor Q2, resistors R4, R6 and R12. When pin 1 of terminal block TB2 is pulled low, a voltage divider to the gate of Q2 is formed between resistors R8 and R4. This drives the gate to source voltage of the P-channel MOSFET switch below its threshold causing it to turn on. Its drain voltage, connected to resistor R4 approaches that of the FET source node which is connected to the positive input voltage (+VIN). Now a voltage divider is activated between the input voltage and ground via R4 and R6 which forces the error amplifier inverting input voltage to rise above the 2.6VDC shutdown threshold, placing the device into its low current standby mode.

Other Applications

Many other voltage step down applications are addressable by the UC3573 Buck Regulator PWM Controller. Following a brief design exercise, the UC3573 Demonstration Kit can be repopulated with the exact components to evaluate other DC to DC converter designs. Consult the UC3573 Datasheet for additional information.